Electronic Version

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Claims

[c1] 1.An oscillator comprising:

an oscillating crystal having a fundamental frequency of oscillation but forced to oscillate at a third overtone of the fundamental frequency, the third overtone being a frequency of about three times the fundamental frequency;

the oscillating crystal coupled between a first input node and a second input node;

a first amplifier circuit having an input attached to the first input node and generating a first output, the first amplifier also having a first phase-shift node;

a second amplifier circuit having an input attached to the second input node and generating a second output, the second amplifier also having a second phase-shift node;

a tuning resistor coupled between the first input node of the first amplifier and the second input node of the second amplifier, the tuning resistor having a value such that an absolute value of a product (gm x Xc1 x Xc2) is greater than an effective impedance of the oscillating crystal, wherein gm is a gain of the first amplifier circuit and gm is also the gain of the second amplifier circuit, and Xc1 is an effective reactance of an equivalent capac-

itance on the first input node of the first amplifier and Xc1 is also an effective reactance of an equivalent capacitance on the second input node of the second amplifier, and Xc2 is an effective reactance of an equivalent capacitance on the first phase-shift node of the first amplifier and Xc2 is also the effective reactance of the equivalent capacitance on the second phase-shift node of the second amplifier;

a multiplier, coupled to the first amplifier circuit and to the second amplifier circuit, for generating a doubled output from the first output and from the second output, the doubled output having an output frequency that is double the third overtone and about six times the fundamental frequency of the oscillating crystal; and

an output filter, attached to the doubled output, for attenuating signals having a frequency of the third overtone, but for passing signals having the output frequency,

whereby the oscillating crystal is forced to oscillate at the third overtone, while the doubled output is six times the fundamental frequency of the oscillating crystal.

[c2] 2.The oscillator of claim 1 wherein the oscillating crystal is a Bulk Acoustic Wave (BAW) crystal resonator.

[c3] 3.The oscillator of claim 2 wherein the first amplifier circuit is a Colpitts oscillator amplifier the second amplifier

circuit is a Colpitts oscillator amplifier, or the first amplifier circuit is a Pierce oscillator amplifier and the second amplifier circuit is a Pierce oscillator amplifier.

[c4] 4.The oscillator of claim 2 wherein the tuning resistor comprises:
a first half-resistor coupled between the first input node and a first inductor node;
a second half-resistor coupled between the second input node and a second inductor node;
an inductor coupled between the first inductor node and the second inductor node.

[c5] 5.The oscillator of claim 2 wherein the first amplifier circuit comprises:
a first transistor having a base connected to the first input node, an emitter driving a first phase-shift node, and a collector driving the first output;
a first source resistor coupled between the first phase-shift node and a ground;
a first phase-shift capacitor coupled between the first phase-shift node and the first input node;
a first additional phase-shift capacitor coupled between the first phase-shift node and the ground;
a first bias circuit, attached to the first input node, for DC-biasing the first input node to a crystal bias voltage;
wherein the second amplifier circuit comprises:

a second transistor having a base connected to the second input node, an emitter driving a second phase-shift node, and a collector driving the second output;
a second source resistor coupled between the second phase-shift node and the ground;
a second phase-shift capacitor coupled between the second phase-shift node and the second input node;
a second additional phase-shift capacitor coupled between the second phase-shift node and the ground;
a second bias circuit, attached to the second input node, for DC-biasing the second input node to a crystal bias voltage;
wherein the multiplier comprises:
a summing node that connects the first output, the second output, and the doubled output together as a single node;
a summing resistor coupled to the summing node, for summing currents from the first amplifier circuit and from the second amplifier circuit,
wherein currents for signals operating at the third overtone are subtracted at the summing node while currents for signals operating at six times the fundamental frequency are added at the summing node.

[c6] 6.The oscillator of claim 2 wherein the first amplifier circuit comprises:

a first transistor having a gate receiving the first input node, with a channel between the first output and a first node;
a first biasing resistor coupled between the first output and the first node;
a first phase-shift capacitor coupled between the first input node and the first node;
a first tail transistor having a gate receiving a reference voltage and a channel between the first node and a ground;
a first additional phase-shift capacitor coupled between the first node and the ground;
wherein the second amplifier circuit comprises:
a second transistor having a gate receiving the second input node, with a channel between the second output and a second node;
a second biasing resistor coupled between the second output and the second node;
a second phase-shift capacitor coupled between the second input node and the second node;
a second tail transistor having a gate receiving the reference voltage and a channel between the second node and the ground;
a second additional phase-shift capacitor coupled between the second node and the ground;
wherein the multiplier comprises:

a summing node that connects the first output and the second output together as a single node;
a summing resistor coupled to the summing node, for summing currents from the first amplifier circuit and from the second amplifier circuit,
wherein currents for signals operating at the third overtone are subtracted at the summing node while currents for signals operating at six times the fundamental frequency are added at the summing node.

[c7] 7.The oscillator of claim 6 wherein the multiplier further comprises:
a DC-filtering capacitor coupled between the summing node and a gate node;
an output transistor having a gate receiving the gate node and a drain driving the doubled output,
whereby the doubled output is capacitively coupled.

[c8] 8.The oscillator of claim 7 wherein the multiplier further comprises:
a gate pull-down resistor coupled between the gate node and the ground;
a pull-up transistor having a gate receiving a second reference voltage, for driving the gate node;
wherein the output filter comprises:
a capacitor coupled between the doubled output and a power supply.

[c9] 9.The oscillator of claim 7 wherein the multiplier further comprises:
a pull-up output transistor, having a gate receiving the gate node and a drain driving the doubled output;
a feedback resistor coupled between the doubled output and the gate node.

[c10] 10.The oscillator of claim 2 wherein the first amplifier circuit comprises:
a first current source driving a current to a first circuit node;
a first cross-coupled transistor having a gate receiving the first circuit node, a drain driving a second lower circuit node, and a source coupled to the first current source at the first circuit node;
a first direct-coupled transistor having a gate receiving a second circuit node, a drain driving a first lower circuit node, and a source coupled to a ground;
wherein the second amplifier circuit comprises:
a second current source driving a current to the second circuit node;
a second cross-coupled transistor having a gate receiving the second circuit node, a drain driving the first lower circuit node, and a source coupled to the second current source at the second circuit node;
a second direct-coupled transistor having a gate receiv-

ing the first circuit node, a drain driving the second lower circuit node, and a source coupled to the ground;
wherein the multiplier comprises:
a third current source driving a current to a third circuit node;
a first multiplier transistor having a gate receiving the first circuit node and a channel between the third circuit node and the doubled output;
a second multiplier transistor having a gate receiving the second circuit node and a channel between the third circuit node and the doubled output.

[c11] 11.The oscillator of claim 10 wherein the first cross-coupled transistor is an n-channel transistor;
wherein the first direct-coupled transistor is an n-channel transistor;
wherein the second cross-coupled transistor is an n-channel transistor;
wherein the second direct-coupled transistor is an n-channel transistor;
wherein the first multiplier transistor is a p-channel transistor; and
wherein the second multiplier transistor is a p-channel transistor.

[c12] 12.The oscillator of claim 10 wherein the multiplier further comprises:

an additional capacitor coupled between the third circuit node and the ground.

[c13] 13.The oscillator of claim 10 wherein the first current source comprises:
a first upper cascode transistor, having a gate receiving an upper bias voltage;
a first lower cascode transistor, having a gate receiving an lower bias voltage;
wherein the first upper cascode transistor and the first lower cascode transistor have channels in series between a power supply and the first circuit node;
wherein the second current source comprises:
a second upper cascode transistor, having a gate receiving an upper bias voltage;
a second lower cascode transistor, having a gate receiving an lower bias voltage;
wherein the second upper cascode transistor and the second lower cascode transistor have channels in series between the power supply and the second circuit node.

[c14] 14.The oscillator of claim 10 further comprising:
a first matched capacitor coupled in a forward layout connection between the first lower circuit node and the second lower circuit node, wherein a positive terminal is connected to the first lower circuit node and a negative terminal is connected to the second lower circuit node;

a second matched capacitor coupled in a reverse layout connection between the first lower circuit node and the second lower circuit node wherein a positive terminal is connected to the second lower circuit node and a negative terminal is connected to the first lower circuit node;;
wherein the first matched capacitor and the second matched capacitor have a same capacitance value between the first lower circuit node and the second lower circuit node but have different parasitic capacitances to the ground for the positive terminal and for the negative terminal.

[c15] 15.The oscillator of claim 10 wherein the first input node and the first circuit node are directly connected together as a same node;
wherein the second input node and the second circuit node are directly connected together as a same node.

[c16] 16.The oscillator of claim 10 further comprising:
a first AC-coupling capacitor between the first input node and the first circuit node;
a second AC-coupling capacitor between the second input node and the second circuit node;
wherein the first input node and the first circuit node are capacitivly coupled together by the first AC-coupling capacitor;
wherein the second input node and the second circuit

node are capacitivly coupled together by the second AC-coupling capacitor.

[c17] 17.The oscillator of claim 16 further comprising:
a second tuning resistor, coupled between the first circuit node and the second circuit node.

[c18] 18.A clock generator comprising:
oscillating crystal means, having a fundamental frequency of oscillation and a third overtone, for oscillating at a third overtone of the fundamental frequency in response to a first crystal node and a second crystal node;
first amplifier means, having the first crystal node as an input, for generating a first output, the first amplifier means having a first node;
second amplifier means, having the second crystal node as an input, for generating a second output, the second amplifier means having a second node;
tuning resistor means, coupled between the first crystal node and the second crystal node, for tuning the clock generator and the oscillating crystal means to oscillate at the third overtone, the tuning resistor means having a value such that an absolute value of a product (gm x Xc1 x Xc2) is greater than an effective impedance of the oscillating crystal means, wherein gm is a gain of the first amplifier means and the gain of the second amplifier means, and Xc1 is an effective reactance of an equivalent

capacitance on the first crystal node or on the second crystal node, and Xc2 is an effective reactance of an equivalent capacitance on the first node or on the second node;

multiplier means, coupled to the first amplifier means and to the second amplifier means, for generating a doubled output from the first output and from the second output, the doubled output having an output frequency that is double the third overtone and about six times the fundamental frequency of the oscillating crystal means; and

output filter means, attached to the doubled output, for attenuating signals having a frequency of the third overtone, but for passing signals having the output frequency,

whereby the oscillating crystal means is forced to oscillate at the third overtone, while the doubled output is six times the fundamental frequency of the oscillating crystal means.

[c19] 19.The clock generator of claim 18 wherein the oscillating crystal means is a Bulk Acoustic Wave (BAW) crystal resonator;

wherein the first amplifier means comprises:

first transistor means, having a gate receiving the first crystal node, for conducting current between the first

output and a first node;
first biasing resistor means, coupled between the first output and the first node, for supplying current to the first node;
first phase-shift capacitor means, coupled between the first crystal node and the first node, for applying an initial phase shift;
first tail transistor means, having a gate receiving a reference voltage, for conducting current from the first node to a ground;
first additional phase-shift capacitor means, coupled between the first node and the ground, for applying an additional phase shift;
wherein the second amplifier means comprises:
second transistor means, having a gate receiving the second crystal node, for conducting current between the second output and a second node;
second biasing resistor means, coupled between the second output and the second node, for supplying current to the second node;
second phase-shift capacitor means, coupled between the second crystal node and the second node, for applying the initial phase shift;
second tail transistor means, having a gate receiving a reference voltage, for conducting current from the second node to the ground;

second additional phase-shift capacitor means, coupled between the second node and the ground, for applying the additional phase shift;
wherein the multiplier means comprises:
summing node means for connecting the first output and the second output together as a single node;
summing resistor means, coupled to the summing node means, for summing currents from the first amplifier means and from the second amplifier means,
wherein currents for signals operating at the third overtone are subtracted by the summing node means while currents for signals operating at six times the fundamental frequency are added by the summing node means;
DC-filtering capacitor means, coupled between the summing node means and a gate node, for blocking DC signals but passing AC signals;
output transistor means, having a gate receiving the gate node and a drain driving the doubled output, for driving the doubled output.

[c20] 20.The clock generator of claim 18 wherein the oscillating crystal means is a Bulk Acoustic Wave (BAW) crystal resonator;
wherein the first amplifier means comprises:
first current source means for driving a current to a first

circuit node;

first cross-coupled transistor means, having a gate receiving the first circuit node, for driving a second lower circuit node from a source coupled to the first current source means at the first circuit node;

first direct-coupled transistor means, having a gate receiving a second circuit node, for driving a first lower circuit node from a source coupled to a ground;

wherein the second amplifier means comprises:

second current source means for driving a current to the second circuit node;

second cross-coupled transistor means, having a gate receiving the second circuit node, for driving the first lower circuit node from a source coupled to the second current source means at the second circuit node;

second direct-coupled transistor means, having a gate receiving the first circuit node, for driving the second lower circuit node from a source coupled to the ground;

wherein the multiplier means comprises:

third current source means for driving a current to a third circuit node;

first multiplier transistor means, having a gate receiving the first circuit node, for conducting current between the third circuit node and the doubled output;

second multiplier transistor means, having a gate receiving the second circuit node, for conducting current be-

tween the third circuit node and the doubled output.